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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,257	07/31/2003	William B. Boyle	K35A1307	4789

35219 7590 11/20/2006

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,257	BOYLE, WILLIAM B.	
	Examiner	Art Unit	
	B. James Peikari	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 21-24, 28-30, 34-37, and 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Grimsrud et al. (US Patent 7,000,077 B2), hereinafter simply Grimsrud.

Regarding claims 21 and 34, Grimsrud teaches a cache control system connectable to a remote memory, the cache control system comprising:

a micro-controller for executing micro-controller data (*note processor 12*);

a buffer manager for arbitrating access to the remote memory (*Fig. 3, storage buffer 46; column 2, lines 9-12*);

a micro-controller cache system coupled to the micro-controller and the buffer manager for fetching and caching micro-controller data stored in the remote memory via

the buffer manager for access by the micro-controller (*Fig. 3, storage cache 50; column 2, lines 17-23*); and

a cache demand circuit (*Fig. 3, micro-controller 40*) coupled to the micro-controller and the micro-controller cache system for receiving an address in the remote memory from the micro-controller and transmitting the address to the micro-controller cache system (*note for example, the "prefetch request" for particular data as in column 2, lines 34-37, or column 6, lines 20-30*);

wherein the micro-controller cache system is responsive to the transmitted address to fetch micro-controller executable data stored at the transmitted address before the micro-controller requests execution of the micro-controller executable data (*column 6, lines 20-38*).

Regarding claims 22-23 and 35-36, Grimsrud teaches a cache control system, wherein the cache demand circuit is further responsive to a memory access signal to transmit the address to the micro-controller cache system (*column 6, lines 20-30*).

Regarding claims 24 and 37, Grimsrud teaches a cache control system, wherein the memory access signal comprises a write signal received from the micro-controller (*column 6, lines 20-38*).

Regarding claims 28 and 40, Grimsrud teaches a cache control system, wherein the cache demand circuit receives the address from the micro-controller before the memory access signal (*column 4, lines 4-21*).

Regarding claims 29, 30, 41, and 42, Grimsrud teaches a cache control system of Claim 22, wherein the cache demand circuit is operable to store the address received from the micro-controller (*column 6, lines 14-30*).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 25-27, 31-33, 38-39, and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grimsrud et al. (US Patent 7,000,077 B2) in view of Hoskins (US Patent 6,789,132 B2).

Regarding claims 25, 26, and 38, Grimsrud teaches a cache control system connectable to a remote memory, the cache control system comprising:

a micro-controller for executing micro-controller data (*note processor 12*);

a buffer manager for arbitrating access to the remote memory (*Fig. 3, storage buffer 46; column 2, lines 9-12*);

a micro-controller cache system coupled to the micro-controller and the buffer manager for fetching and caching micro-controller data stored in the remote memory via the buffer manager for access by the micro-controller (*Fig. 3, storage cache 50; column 2, lines 17-23*); and

a cache demand circuit (*Fig. 3, micro-controller 40*) coupled to the micro-controller and the micro-controller cache system for receiving an address in the remote memory from the micro-controller and transmitting the address to the micro-controller cache system (*note for example, the "prefetch request" for particular data as in column 2, lines 34-37, or column 6, lines 20-30*);

wherein the micro-controller cache system is responsive to the transmitted address to fetch micro-controller executable data stored at the transmitted address before the micro-controller requests execution of the micro-controller executable data (*column 6, lines 20-38*).

Grimsrud fails to explicitly mention interrupting the micro-controller based on a transmitted interrupt signal. However, Hoskins teaches an interrupt circuit adapted to interrupt the micro-controller based on a transmitted interrupt signal (*See, Fig. 2, element 230, host interrupt module; column 10, lines 56-67*). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Grimsrud with Hoskins. It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement Grimsrud's pre-fetch with Hoskins' interrupt, since (1) this would minimize delays and (2) would have provided efficient management of data transfers with an interrupt protocol and (3) Hoskins states why the inclusion of such a feature would be beneficial: the preemptive control modules are for handling time critical operations, such as responses to interrupts from a host computer (*column 3, lines 5-7*).

Regarding claims 27 and 39, Hoskins teaches a cache control system, wherein the micro-controller executable data fetched by the micro-controller cache system is executed by the micro-controller during a micro-controller interrupt service routine (*column 25, lines 31-43*).

Regarding claims 31 and 43, Hoskins teaches a cache control system, wherein the memory access signal comprises a servo-interrupt signal (*column 10, lines 56-67*).

Regarding claims 32 and 44, Hoskins teaches a cache control system of Claim 22, wherein the memory access signal comprises a host-interrupt signal (*Fig. 2, element 230, host interrupt module; column 10, lines 56-67*).

Regarding clams 33, Hoskins teaches a cache control system, wherein the buffer manager is in communication with a plurality of disk drive control system clients, including at least one of a disk subsystem, an error correction code subsystem, and a host interface subsystem (*column 30, lines 59-66*).

Response to Arguments

5. Applicant's arguments filed 5/26/2006 have been fully considered but they are not persuasive.

(A) These arguments are moot in view of the revisions presented above.

(B) It is noted that a microprocessor (such as processor 12) is a micro-controller.

(C) Note that the prefetch scheme of Grimsrud et al. may include a "prefetch request" that is sent before any "official" request for the data and, contrary to applicant's remarks on page 3, the actual data that is needed may be requested during the prefetch, not just data that is "derived" from the actual data.

(D) In fact, there is nothing in applicant's specification that teaches anything other than the embodiment described in (C) above. For example, applicant

argues that in the present invention, data is fetched before a request is made. This is not correct.

In applicant's specification, such a fetch is performed by the receipt of "memory address 214a and a memory access signal 214b from the micro-controller 204" (note paragraph [00015]). If this is not a request, then what is? Contrary to applicant's assertions a memory access signal *is* a request, albeit a prefetch request.

Thus, applicant's invention issues a prefetch request, and so does the system of Grimsrud et al.

Consequently, every feature of the present claims is either taught or suggested by Grimsrud et al. or by the Grimsrud et al./ Hoskins combination described above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

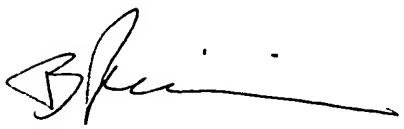
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached at (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center at 866-217-9197 (toll-free).



B. James Peikari
Primary Examiner
Art Unit 2189
11/12/06